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J. Daniell, S. W. Director

June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**Full text available:  [pdf\(808.85 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

As VLSI design frameworks evolve, a distributed control mechanism for CAD tools has become a central research issue. In this paper, we present an object oriented tool integration methodology that treats the tools as objects. This approach simplifies CAD tool control within a design framework making the framework more general, easier to use, and more capable of supporting a large population of CAD tools.

2 CAD methodology for the design of UltraSPARC-I microprocessor at Sun Microsystems Inc.

A. Cao, A. Adalal, J. Bauman, P. Dedood, P. Donehue, P. Delisle, M. Dell'OcaKhouja, T. Doan, M. Doreswamy, P. Ferolito

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**Full text available:  [pdf\(265.70 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)**3 Computer aided design (CAD) using logic programming**

Paul W. Horstmann, Edward P. Stabler

June 1984 **Proceedings of the 21st conference on Design automation**Full text available:  [pdf\(627.26 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper gives an overview of expert systems and logic programming as applied to Computer-Aided Design (CAD) systems. Our objective is to show the relevance of these two approaches developed from research in artificial intelligence for the solution of problems in VLSI design. We will provide some examples of the use of logic programming for familiar CAD tasks. The expert systems discussed function as experts in a very narrowly defined area of expertise, and can be called designer's assist ...

Keywords: Artificial intelligence, Computer-aided design, Logic programming

4 MIDAS: integrated CAD for total system design

W. M. Budney, S. K. Holewa

June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**Full text available:  pdf(693.92 KB)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Control Data's Modular Integrated Design Automation System (MIDAS) is a highly integrated CAD system supporting the full range of activities required for the design of complex digital systems. From schematic capture through design verification and manufacturing, MIDAS emphasizes a structured top down approach, from chips to supercomputers. MIDAS is fully hierarchical and is capable of managing and controlling the design of some of the world's largest computers, as well as speeding up the de ...

5 Reduced design time by load distribution with CAD framework methodology information

Jürgen Schubert, Arno Kunzmann, Wolfgang Rosenstiel

December 1995 **Proceedings of the conference on European design automation**Full text available:  pdf(700.73 KB)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)**6 DDB: an object oriented design data manager for VLSI CAD**

Anoop Singhal, Robert M. Arlein, Chi-Yuan Lo

June 1993 **ACM SIGMOD Record , Proceedings of the 1993 ACM SIGMOD international conference on Management of data**, Volume 22 Issue 2Full text available:  pdf(170.90 KB)Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper we present an object oriented data model for VLSI/CAD data. A design data manager (DDB) based on such a model has been implemented under the UNIX/C++ environment. It has been used by a set of diverse VLSI/CAD applications of our organization. Benchmarks have shown it to perform better as compared to commercial object oriented database systems. In conjunction with the ease of data access, the data manger served to improve software productivity and a modular program architecture ...

7 The role of VHDL in the MCC CAD system

Ramón D. Acosta, Mark Alexandre, Gary Imken, Bill Read

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**Full text available:  pdf(753.39 KB)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The VHSIC Hardware Description Language (VHDL), currently undergoing standardization by the IEEE, supports the hierarchical design, documentation, and simulation of a wide range of digital system abstractions. This paper describes a suite of utilities for manipulating VHDL designs that has been developed and integrated into the CAD System of the Microelectronics and Computer Technology Corporation (MCC). The MCC CAD System is a tightly integrated environment supporting the sharing of design ...

8 Design technology research for the nineties: more of the same?

H. de Man

November 1992 **Proceedings of the conference on European design automation**Full text available:  pdf(478.66 KB)Additional Information: [full citation](#), [citations](#), [index terms](#)**9 QCADS-a LSI CAD system for minicomputer**

Hong Xian-long, Yin Ren-kung, Liu Xi-ling

January 1982 Proceedings of the 19th conference on Design automation

Full text available:  pdf(431.53 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The computer aided design (CAD) technique for LSI is an indispensable tool to develop LSI. Setting up a LSI CAD system with center on CAD database would make CAD technique more effectual. And a LSI CAD system for minicomputer has advantages of lower cost and convenient management. In this paper we are concerned with describing effective LSI CAD system - QCADS for minicomputer. The paper consists of four parts: (1) design objectives and strategy of the system, (2) framework of the ...

10 Modeling concepts for VLSI CAD objects 

D. S. Batory, Won Kim

September 1985 **ACM Transactions on Database Systems (TODS)**, Volume 10 Issue 3

Full text available:  pdf(1.76 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

VLSI CAD applications deal with design objects that have an interface description and an implementation description. Versions of design objects have a common interface but differ in their implementations. A molecular object is a modeling construct which enables a database entity to be represented by two sets of heterogeneous records, one set describes the object's interface and the other describes its implementation. Thus a reasonable starting point for modeling design objects is to begin w ...

11 Knowledge based approach for the verification of CAD database generated by an automated schematic capture system 

J. Y. Tou, W. H. Ki, K. C. Fan, C. L. Huang

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available:  pdf(765.41 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

CAD database generated by an automatic schematic capture system needs to be verified before it can be used in design automation. This verification is best performed by a knowledge-based expert system. Presented in this paper is the design of a knowledge-based system for the verification of CAD database generated by AUTORED. Database-driven, pattern-directed inference technique is employed to identify and correct erroneous data records due to misrecognition. This knowledge-based verification ...

12 Computer aided design and design automation in Europe 

Waldo G. Magnuson

June 1976 **ACM SIGDA Newsletter**, Volume 6 Issue 2

Full text available:  pdf(884.88 KB) Additional Information: [full citation](#), [abstract](#)

The development of CAD and DA in Italy and Germany compares closely with that in Britain. Germany, although lagging behind the US in computer utilization in engineering design, appeared to have better and more numerous contacts with US research in CAD and DA than either Italy or Britain has. Philips in Holland is taking a very aggressive approach to developing company coordination in CAD. Similarly, Siemens in Germany has a sizable group in CAD. Olivetti in Italy over the years, has developed ex ...

13 Thick film substrate (Micropackage) design utilizing interactive Computer Aided Design systems 

Freddie M. Christley

January 1977 **Proceedings of the 14th conference on Design automation**

Full text available:  pdf(772.78 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Honeywell Information System, Inc. in Phoenix, Arizona utilizes Computer Aided Design (CAD) systems with graphics capabilities and online data bases to design, build and test

thick film substrates. The thick film substrate is enclosed in a metal housing with edge connections and is called a Micropackage.

14 Interconnect scaling implications for CAD

Ron Ho, Ken Mai, Hema Kapadia, Mark Horowitz

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available:  pdf(91.68 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Interconnect scaling to deep submicron processes presents many challenges to today's CAD flows. A recent analysis by Sylvester and Keutzer examined the behavior of average length wires under scaling, and controversially concluded that current CAD tools are adequate for future module-level designs. In our work, we show that average length wire scaling is sensitive to the technology assumptions, although the change in their behavior is small under all reasonable scaling assumptions. H ...

15 Conceptual graphs in constraint based re-design

O. W. Salomons, F. van Slooten, F. J. A. M. van Houten, H. J. J. Kals

December 1995 **Proceedings of the third ACM symposium on Solid modeling and applications**

Full text available:  pdf(1.08 MB)

Additional Information: [full citation](#), [references](#), [index terms](#)

Keywords: CAD, CAPP, conceptual graphs, constraints, features, re-design

16 Automated design based upon Microprogrammable Bit Slice Microprocessors

Bernard J. Carey, George F. MacLachlan

February 1977 **Proceedings of the Symposium on Design Automation and Microprocessors**

Full text available:  pdf(376.93 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This article will discuss an automated approach to designing digital systems which is based upon the use of System Description Languages (SDL)1,2,3 and Microprogrammable Bit Slice Microprocessors (MBSM)4,5. Both of these concepts have started to reach maturity in recent years with the result that Computer Aided Design (CAD) systems6,7,8 are starting to evolve to a level whereby they may be truly useful in automating certain of t ...

17 The effects of CAD on the engineering organization (Position paper)

Paul Felton

June 1981 **Proceedings of the 18th conference on Design automation**

Full text available:  pdf(198.86 KB)

Additional Information: [full citation](#), [abstract](#), [index terms](#)

The growth in the use of Computer Aided Design (CAD) tools within the Engineering organization has been an evolutionary process. CAD technology has progressed from isolated analysis and documentation tools into complete integrated CAD systems. In order for an Engineering organization to effectively use an integrated CAD system, changes have to be made to organizational structure, organizational interfaces, project funding and project scheduling methodologies.

18 An overview of the Penn State design system

R. M. Owens, M. J. Irvin

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available:

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index](#)

[!\[\]\(2e897e890e69d81eae4503a8342c36b0_img.jpg\) pdf\(840.54 KB\)](#)[terms](#)

This paper overviews a CAD system under development at Penn State which will allow fast and near optimal implementation of a restricted class of VLSI architectures. Our target architectures are hierarchical mesh extensions of systolic meshes. Our target applications are primarily in the signal processing domain. The primitive components, at the lowest level in the mesh hierarchy, are one of the unique features of our target architectures. The CAD system under development includes: a tool fo ...

19 [Design management using dynamically defined flows](#)

Peter R. Sutton, Jay B. Brockman, Stephen W. Director

July 1993 **Proceedings of the 30th international conference on Design automation**

Full text available: [!\[\]\(0b5e7e25e8775f7e7e80906ada4f0021_img.jpg\) pdf\(734.93 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

20 [Assessing the effect of non-photorealistic rendered images in CAD](#)

Jutta Schumann, Thomas Strothotte, Stefan Laser, Andreas Raab

April 1996 **Proceedings of the SIGCHI conference on Human factors in computing systems: common ground**

Full text available: [!\[\]\(bd3b31712ad9bab5a241210fa6925cdd_img.jpg\) pdf\(860.38 KB\)](#) [!\[\]\(882be629d4a853dc90d60f084b0d185d_img.jpg\) html\(26.38 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: CAD, architectural presentation, non-photorealistic rendering, preliminary drafts, sketches

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1 [TimeBench: a CAD tool for real-time system design](#)

R. J. A. Buhr, G. M. Karam, C. M. Woodside, R. Casselman, G. Franks, H. Scott, D. Bailey
 September 1994 **ACM SIGAda Ada Letters , Proceedings of the second international symposium on Environments and tools for Ada**, Volume XIV Issue SI

Full text available: [pdf\(1.18 MB\)](#) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

This paper provides an overview of *TimeBench*, a prototype CAD tool for designing real-time systems, as well as some experiences gained through building and using it. *TimeBench* aims to support a true engineering design process for real-time systems in a largely graphical working environment. The environment includes support for design synthesis, analysis, and system generation, with equal emphasis on the design of operational structure and the design of temporal behavior. Its main features ...

2 [On the use of VHDL-based behavioral synthesis for telecom ASIC design](#)

Mark Genoe, Paul Vanoostende, Geert van Wauwe
 September 1995 **Proceedings of the 8th international symposium on System synthesis**

Full text available: Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)
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Abstract: VHDL-based behavioral synthesis is appearing on the market but it still has to prove that it can have a significant impact. In the past, most applications for behavioral synthesis came from the DSP area and from the academic world. In contrast, this paper describes the results of an investigation and evaluation of several behavioral synthesis tools, carried out on recent designs of Alcatel-Bell, leading to a more detailed study of relevant industrial telecom non-DSP circuits, that were ...

Keywords: Alcatel-Bell, RTL-synthesizable description, VHDL, application specific integrated circuits, behavioral synthesis, behavioral synthesis tools, design complexities, hardware CAD tool, hardware description languages, hardware software codesign, high level synthesis, integrated circuit design, integrated logic circuits, logic synthesis, system level design methodology, telecom ASIC design, telecom system hardware design, telecommunication computing

3 [An evolution programming approach on multiple behaviors for the design of application specific programmable processors](#)

Wei Zhao, C. A. Papachristou
 March 1996 **Proceedings of the 1996 European conference on Design and Test**

Full text available:  pdf(819.57 KB)

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Additional Information: [full citation](#), [abstract](#), [citations](#)

This paper proposes an Evolution Programming Approach for behavior-level area-efficient design of ASPPs (Application Specific Programmable Processors). This approach, based on a given behavioral-level kernel, randomly transforms each of the input behaviors, then the behavioral kernel is used in the evolution process to guide the survival of data flow graphs (DFGs). Finally, instead of the given DFGs, the surviving DFGs are used to synthesize a programmable architecture. This leads to an area-eff ...

Keywords: DSP chips, application specific integrated circuits, application specific programmable processors, area-efficient design, behavior-level area-efficient design, behavioral kernel, circuit CAD, circuit layout CAD, data flow graphs, digital signal processing chips, evolution programming approach, high level synthesis, integrated circuit design, logic design, multiple behaviors, programmable architecture, programming

4 CORAL II: linking behavior and structure in an IC design system

Robert L. Blackburn, Donald E. Thomas, Patti M. Koenig

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

Full text available:  pdf(929.51 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper describes a technique for maintaining very fine grained links between a behavioral specification and an automatically generated VLSI structural implementation. CORAL II exceeds previous systems in the scope of design representations involved and the complexity of the relationships handled. The design representations used are described, as are the behavioral transformations that may be applied and the types of design choices that may be made. The complications introduced by these ...

5 Methodology for behavioral synthesis-based algorithm-level design space exploration:

DCT case study

Miodrag Potkonjak, Kyosun Kim, Ramesh Karri

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available:  pdf(363.01 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

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Numerous fast algorithms for the DiscreteCosine Transform (DCT) have been proposed. Until recently, it has been difficult to compare different DCT algorithms and select one which is best suited for implementation under a given set of design goals. We propose an approach for design space exploration at the algorithm and behavioral levels using behavioral synthesis tools and demonstrate its effectiveness for designing DCT ASIC. In particular, we study and compare the following nine DCT algorithms: Lee ...

6 Electronically-mediated partnerships: the use of CAD technologies in supplier relations

M. Bensaou

January 1999 **Proceeding of the 20th international conference on Information Systems**

Full text available:  pdf(238.89 KB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

7

Vertical benchmarks for CAD

Christopher Inacio, Herman Schmit, David Nagle, Andrew Ryan, Donald E. Thomas, Yingfai

Tong, Ben Klass

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available:  pdf(90.16 KB)

Additional Information: [full citation](#), [references](#), [index terms](#)

8 From VHDL to efficient and first-time-right designs: a formal approach 

Peter F. A. Middelhoek, Sreeranga P. Rajan

April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**,
Volume 1 Issue 2

Full text available:  pdf(722.99 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this article we provide a practical transformational approach to the synthesis of correct synchronous digital hardware designs from high-level specifications. We do this while taking into account the complete life cycle of a design from early prototype to full custom implementation. Besides time-to-market, both flexibility with respect to target architecture and efficiency issues are addressed by the methodology. The utilization of user-selected behavior-preserving transformation steps e ...

Keywords: CDFG, SFG, VHDL, correctness by construction, design methodology, rapid system prototyping, transformational design

9 Paper session #2: Naturally conveyed explanations of device behavior 

Michael Oltmans, Randall Davis

November 2001 **Proceedings of the 2001 workshop on Perceptive user interfaces PUI '01**

Full text available:  pdf(182.86 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Designers routinely explain their designs to one another using sketches and verbal descriptions of behavior, both of which can be understood long before the device has been fully specified. But current design tools fail almost completely to support this sort of interaction, instead not only forcing designers to specify details of the design, but typically requiring that they do so by navigating a forest of menus and dialog boxes, rather than directly describing the behaviors with sketches and ve ...

10 A design flow for partially reconfigurable hardware 

Ian Robertson, James Irvine

May 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 2

Full text available:  pdf(698.30 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents a top-down designer-driven design flow for creating hardware that exploits partial run-time reconfiguration. Computer-aided design (CAD) tools are presented, which complement conventional FPGA design environments to enable the specification, simulation (both functional and timing), synthesis, automatic placement and routing, partial configuration generation and control of partially reconfigurable designs. Collectively these tools constitute the dynamic circuit switching CAD f ...

Keywords: FPGA, Viterbi decoder, configuration control, dynamically reconfigurable logic (DRL), power estimation, run-time reconfiguration (RTR)

11 Incorporating the human factor in color CAD systems 

Francine S. Frome

June 1983 **Proceedings of the 20th conference on Design automation**

Full text available:  pdf(1.34 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Computer Aided Design (CAD) systems require the presentation of visual information of various kinds to users at workstations. This paper discusses how to make use of user studies and behavioral research to design more effective and productive CAD systems. Topics include: • optimizing the color display of printed wiring boards, violations, messages, and menus; • increasing workstation productivity by taking advantage of the characteristics of the human user; a ...

Keywords: Abbreviations, Color, Color vision, Computer aided design, Computer command menus, Ergonomics, Human engineering, Human factors, Human performance, User interface, Visual display terminals, Workstations

12 Defining and implementing a multilevel design representation with simulation applications



J. A. Nestor, D. E. Thomas

January 1982 **Proceedings of the 19th conference on Design automation**

Full text available:  pdf(711.93 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

A design representation that incorporates descriptions at more than one level of abstraction is called a multilevel representation. This paper describes a multilevel representation which includes behavioral and structural levels of description, and a multilevel analysis aid, called timing abstraction, which extracts timing information from a structural design and adds it to a behavior level description. With this design aid, alternate implementations of the same behavior, generated using th ...

13 NES: the behavioral model for the formal semantics of a hardware design language UDL/I



Nagisa Ishiura, Hiroto Yasuura, Shuzo Yajima

January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available:  pdf(731.61 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper describes a new behavioral model of hardware, named NES (Nondeterministic Event Sequence) model, which was developed for the purpose of defining formal semantics of the gate level and the register transfer level hardware description languages. The NES model is a generalization of the event driven simulation, and can be a basis of synthesis and verification as well as simulation. We introduce basic concepts, formal definition, and a description method of the NES model.

14 An intermediate representation for behavioral synthesis



Nikil D. Dutt, Tedd Hadley, Daniel D. Gajski

January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available:  pdf(728.22 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper describes an intermediate representation for behavioral and structural designs that is based on annotated state tables. It facilitates user control of the synthesis process by allowing specification of partially design structures, and a mixture of behavior, structure and user specified bindings between the abstract behavior and the structure. The format's general model allows the capture of synchronous and asynchronous behavior, and permits hierarchical descriptions with concurre ...

15 Incorporating the human factor in color CAD systems



F. S. Frome

June 1988 Papers on Twenty-five years of electronic design automationFull text available:  pdf(636.39 KB) Additional Information: [full citation](#), [references](#), [index terms](#)**16 Behavioral synthesis: Coordinated transformations for high-level synthesis of high performance microprocessor blocks**

Sumit Gupta, Nick Savoiu, Nikil Dutt, Rajesh Gupta, Alex Nicolau, Timothy Kam, Michael Kishinevsky, Shai Rotem

June 2002 Proceedings of the 39th conference on Design automationFull text available:  pdf(144.01 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

High performance microprocessor designs are partially characterized by functional blocks consisting of a large number of operations that are packed into very few cycles (often single-cycle) with little or no resource constraints but tight bounds on the cycle time. Extreme parallelization, conditional and speculative execution of operations is essential to meet the processor performance goals. However, this is a tedious task for which classical high-level synthesis (HLS) formulations are inadequate ...

Keywords: high-level synthesis, microprocessor design**17 The FSM network model for behavioral synthesis of control-dominated machines**

Wayne Wolf

January 1991 Proceedings of the 27th ACM/IEEE conference on Design automationFull text available:  pdf(674.30 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Since many ASICs are dominated by control functions, control-dominated architectures form an important domain for behavioral synthesis. We propose modeling control-dominated architectures during behavioral synthesis as networks of communicating FSMs—the model more directly reflects behavior and allows more accurate cost estimation, especially for control, than do traditional data-directed representations for control-dominated machines. We show how to implement a number of important co ...

**18 SLIF: a specification-level intermediate format for system design**

F. Vahid, D. D. Gajski

March 1995 Proceedings of the 1995 European conference on Design and TestFull text available:  pdf(681.04 KB) Additional Information: [full citation](#), [abstract](#), [citations](#)
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As methodologies and tools for chip-level design mature, design effort becomes focused on higher abstraction levels. Presently, much effort is focused on system-level design, where the key tasks include system component allocation, functional partitioning and transformation, and coarse estimation. However, commonly-used internal formats of functionality, such as the control-dataflow graph, are too fine-grained for the system level. We introduce a more abstract format, and we demonstrate its use ...

Keywords: ASIC, CAD, SLIF, SpecSyn system design environment, application specific integrated circuits, circuit CAD, digital integrated circuits, integrated circuit design, logic CAD, specification-level intermediate format, system-level design**19 Design of system interface modules**

Jane S. Sun, Robert W. Brodersen